

1 **METHOD OF DETERMINING DC MARGIN OF A LATCH**

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10 **Technical Field**

11 The invention relates to electronic circuits. More particularly, the invention relates to simulation
12 and determination of design parameters of an electronic circuit.

13

14 **Background Art**

15 A latch is a circuit element that maintains a particular state between state changing events, i.e.,
16 in response to a particular input, and is ubiquitous in digital sequential circuit designs. For example, as
17 shown in Fig. 1, a typical latch 100 may include, inter alia, a forward inverter 101, a feedback inverter
18 102, an input terminal 103 and an output terminal 104. The output voltage level, V_{OUT} , remains at a
19 particular voltage level, i.e., either high or low, until an input signal, V_{IN} , is received at the input terminal
20 103, at which time the state of the output may change depending on the nature of the input signal. For
21 example, the state of the output 104 may change from a high state to a low state upon receipt of a
22 logical high signal at the input 103.

23 In order for the latch to operate properly, i.e., to change state upon receiving a particular input,
24 the input signal levels to the latch must exceed certain thresholds with a sufficient margin. To this end,
25 during a circuit design, it must be ensured that the input signal levels delivered through various signal
26 paths to each of latches in the circuit under design meet the above input signal margin.

27 One of the ways to ensure satisfaction of the above input signal level requirement is to determine
28 what is often referred to as the "DC margin" for each of the latches present in the circuit being designed.

1 The DC margin is a pair of values, the one margin and the zero margin. The one margin is the difference
2 between the trip voltage (V_{trip}) of the forward inverter **101** of the latch **100** and the worst case pull-up
3 input signal level that may be presented to the latch. The zero margin is the difference between the V_{trip}
4 of the forward inverter **101** and the worst case pull-down input signal level that may be presented to
5 the latch **100**. The trip voltage V_{trip} is defined as the equilibrium voltage level of the output voltage level
6 and the input voltage level of the forward inverter. In order for a particular circuit design to be deemed
7 acceptable, the DC margin must exceed a minimum margin according to a design guideline.

8 Unfortunately, heretofore, in order to determine the DC margin of a latch, every possible signal
9 paths from each of the possible circuit elements that may drive the latch must be examined, requiring
10 performance of simulations, using a simulation program, e.g., the SPICE™, for each of the possible
11 signal paths. The prior attempts to determine the DC margin requires numerous simulations, each of
12 which takes a long time to perform, and are thus inefficient and time consuming. This problem may be
13 exacerbated if there are numerous latches in the particular circuit under design.

14 Thus, there is a need for more efficient method of determining DC margin of a latch, which does
15 not require numerous simulations for every possible signal paths to the latch.

16

17 Summary of Invention

18 In accordance with the principles of the present invention, a method of determining a DC
19 margin of a latch comprises performing a first simulation using a first simulation circuit to determine a
20 trip voltage of a forward inverter of the latch, performing a second simulation using a second simulation
21 circuit to determine a one margin of the latch, the second simulation circuit comprising a worst case pull-
22 up signal path, and performing a third simulation using a third simulation circuit to determine a zero
23 margin of the latch, the third simulation circuit comprising a worst case pull-down signal path .

24 In accordance with another aspect of the principles of the present invention, a computer
25 program stored on a computer readable storage medium implements a method of determining a DC
26 margin of a latch, and comprises a set of instructions for performing a first simulation using a first
27 simulation circuit to determine a trip voltage of a forward inverter of the latch, performing a second
28 simulation using a second simulation circuit to determine a one margin of the latch, the second simulation

1 circuit comprising a worst case pull-up signal path, and performing a third simulation using a third
2 simulation circuit to determine a zero margin of the latch, the third simulation circuit comprising a worst
3 case pull-down signal path .

4 In yet another aspect of the principles of the present invention, a simulation circuit for
5 determining a DC margin of a latch comprises a latch portion representing the latch being simulated, the
6 latch portion comprising a forward inverter and a feedback inverter, an input of the forward inverter
7 being operably connected to an input of the latch portion, and an input of the feedback inverter being
8 operably connected to an output of the latch portion, a driver portion representing a driver circuit
9 element capable of supplying an input signal to the latch being simulated, and a pass path subcircuit
10 configured to receive a drive signal from the driver portion, and configured to supply the drive signal
11 to the input of the latch portion, the pass path subcircuit representing one or more pass circuit elements
12 along a worst case signal path between the driver circuit element and the latch being simulated.

13

14 Description of Drawings

15 Features and advantages of the present invention will become apparent to those skilled in the
16 art from the following description with reference to the drawings, in which:

17 Figure 1 is a logic diagram of showing the relevant portions of a conventional latch.

18 Figure 2 is a circuit diagram illustrative of an embodiment of a simulation model circuit of the
19 a latch and the corresponding input signal path to the latch in accordance with the principles of the
20 present invention;

21 Figure 2A is a circuit diagram illustrative of an embodiment of the path subcircuit shown in Fig.
22 2;

23 Figure 3 is flow diagram illustrative of an exemplary embodiment of the process of determining
24 the DC margin of a latch in accordance with an embodiment of the principles of the present invention;

25 Figure 4 is a circuit diagram illustrative of an embodiment of a simulation circuit for determining
26 the trip voltage of a forward inverter of a latch in accordance with the principles of the present
27 invention;

1 Figure 5 is a circuit diagram illustrative of an embodiment of a simulation circuit for determining
2 the one margin of a latch in accordance with the principles of the present invention; and

3 Figure 6 is a circuit diagram illustrative of an embodiment of a simulation circuit for determining
4 the zero margin of a latch in accordance with the principles of the present invention.

5

6 Detailed Description of Preferred Embodiments

7 For simplicity and illustrative purposes, the principles of the present invention are described by
8 referring mainly to an exemplar embodiment, particularly, with a specific exemplary implementations
9 of various simulation circuits. However, one of ordinary skill in the art would readily recognize that the
10 same principles are equally applicable to, and can be implemented in, other implementations and
11 designs using any other equivalent simulation circuits, and that any such variation would be within such
12 modifications that do not depart from the true spirit and scope of the present invention.

13 In accordance with the principles of the present invention, a DC margin of a latch of a circuit
14 under design is determined by performing three simulations. A simulation is performed to find the trip
15 voltage of the forwarding inverter of the latch. A second simulation is performed to find the one margin
16 of the latch. Lastly, a third simulation is performed to find the zero margin of the latch.

17 During each of the simulations to find the one margin and the zero margin, the worst case input
18 signal path from the various driver circuit elements and signal paths within the circuit under design is
19 determined analytically by accumulating weighted resistance of each of the circuit elements along the
20 signal paths. The weights assigned to the circuit elements are empirically determined based on the
21 topology configuration of each of the circuit elements, e.g., the type circuit element, the signal being
22 passed through the circuit element and whether a threshold voltage drop occurs between the drive
23 circuit element and the pass circuit element.

24 In particular, Fig. 2 shows a simulation model circuit **200** representing a latch and its input signal
25 path in accordance with an embodiment of the present invention. The simulation model circuit
26 represents an equivalent circuit model of the actual circuit being simulated, and may not include every
27 circuit elements present in the actual circuit being simulated. For example, the NFET Q1 **201** may
28 represent more than one circuit element, e.g., a series of NFETs, of the actual circuit being simulated.

1 It should be understood by those familiar with circuit evaluation techniques that each of circuit elements
2 shown in the model circuit 200 shown in Fig. 2 may be an equivalent circuit of, and represent, a
3 number of circuit elements of the actual circuit under simulation.

4 The simulation model circuit comprises a latch model 100', which includes two complementary
5 field effect transistor (FET) pairs, each representing the forward inverter and the feedback inverter of
6 the latch. The complementary pair Q1 201 and Q2 202 together represent the forward inverter while
7 the complementary pair Q3 203 and Q4 204 represent the feedback inverter.

8 The model circuit 200 further comprises a path subcircuit 207 which represent the various
9 circuit elements along a signal path between the input 103 of the latch and a circuit element that may
10 drive the input of the latch. The circuit element that drives the input of the latch is represented by the
11 FETs Q5 205 and Q6 206, each providing a pull-down input signal and a pull-up input signal,
12 respectively, to the input of the latch (i.e., Vin 103) through the path subcircuit 207. As shown, when
13 a logical low signal V_{INH} 208 is supplied to the gate of the PFET Q6 206, the PFET Q6 206 is turned
14 on, and thus Vin 103 is driven high. When a logical high signal V_{INL} 208 is supplied to the gate of the
15 NFET Q5 205, the PFET Q5 205 is turned on, and thus Vin 103 is driven low.

16 Fig. 2A shows the path subcircuit 207 in more detail. According to an embodiment of the
17 present invention, the path subcircuit 207 comprises n/2 complementary pairs of FETs, Q_{S1} to Q_{Sn} ,
18 each of which can be configured to have variable size, and can be individually removed from the path
19 subcircuit 207, to simulate the worst case pull-up and pull-down signal paths. In a preferred
20 embodiment of the present invention, the path subcircuit 207 comprises six (6) complementary pairs
21 of FETs.

22 In an embodiment of the present invention, the worst case pull-up and pull-down signal paths
23 are determined analytically by traversing through each of possible signal paths from the input of the latch
24 to each of circuit elements that can drive the input of the latch, and identifying pass circuit elements
25 along each of the signal paths, through which a signal may pass. For each of identified pass circuit
26 elements, a weight is applied to its resistance, e.g., based on its length and width (L/W). The weights
27 applied to the resistance of the pass circuit elements are empirically determined based on the topology
28 configuration of each of the circuit elements, e.g., the pass circuit element type (e.g., whether the pass

1 circuit element is a single NFET, single PFET or a complementary pair of FETs), the signal being
2 passed through the pass circuit element and whether a threshold voltage drop occurs between the drive
3 circuit element and the pass circuit element.

4 The weighted resistance of the identified pass circuit elements along a particular signal path are
5 added together to determine the total resistance of the particular signal path, and is compared to the
6 total resistance similarly calculated for other signal paths to determine the worst case signal path which
7 results in the worst degradation of signal level while passing through the signal path.

8 In a preferred embodiment of the present invention, the path subcircuit 207 is configured to
9 include one or more of the FETs, Q_{S1} and Q_{S2} , each included FET representing identified pass circuit
10 elements. The sizes of the included FETs in the path subcircuit 207 are based on the sizes of the
11 respective pass circuit elements. In an alternative embodiment, the path subcircuit 207 may simply be
12 a resistor element having the weighted total resistance of the worst case signal path identified.

13 The inventive process of determining DC margin of a latch will now be described with
14 references to FIGs. 4 through 6. In step 301, a simulation, e.g., using SPICE™ which is known to
15 those familiar with circuit design testing, is performed to determine the trip point voltage (V_{trip}) of the
16 forward inverter of the latch. An exemplary embodiment of the simulation circuit 400 for the V_{trip}
17 determination is shown in Fig. 4. In this example, the simulation circuit 400 includes the forward
18 inverter portion of the latch, and comprises the complementary pair of FETs, Q1 201 and Q2 202.

19 As shown, in the simulation circuit 400, the input terminal Vin 103 and the output terminal Vout
20 104 of the forward inverter are connected together. The simulation comprises a DC analysis of the
21 simulation circuit 400 to determine the settling voltage level at the input terminal Vin 103, which is the
22 same as the voltage level at the output terminal Vout 104. Once the voltage levels at the input terminal
23 and the output terminal settles to equal each other, the settling voltage is the trip point voltage (V_{trip}) of
24 the forward inverter of the latch.

25 In step 302, the worst case pull-up signal path and the path subcircuit 207 based on the worst
26 case pull-up signal path are found as previously described. In particular, in an embodiment of the
27 present invention, the worst case pull-up signal path is determined analytically by traversing through
28 each of possible signal paths from the input of the latch to each of pull-up driver circuit elements that

1 can drive a pull-up signal to the input of the latch, and identifying pass circuit elements along each of
2 the signal paths, through which a signal may pass. For each of identified pass circuit elements, a weight
3 is applied to its resistance, e.g., based on its length and width (L/W). The weights applied to the
4 resistance of the pass circuit elements are empirically determined based on the topology configuration
5 of each of the circuit elements, e.g., the pass circuit element type (e.g., whether the pass circuit element
6 is a single NFET, single PFET or a complementary pair of FETs), the signal being passed through the
7 pass circuit element and whether a threshold voltage drop occurs between the pull-up driver circuit
8 element and the pass circuit element.

9 The weighted resistance of the identified pass circuit elements along a particular signal path are
10 added together to determine a cumulative resistance of the particular signal path, i.e., from the supply
11 voltage V_{DD} through the pull-up driver circuit element and the pass circuit elements to the latch input.
12 The cumulative resistance of each signal path is compared to the total resistance similarly calculated for
13 other signal paths to determine the worst case pull-up signal path, i.e., the signal path with the highest
14 cumulative resistance, which results in the worst degradation of signal level while passing through the
15 signal path.

16 The pull-up driver of the identified worst case pull-up signal path is mapped to an equivalent
17 canonical driver circuit Q6 206 as shown in Fig. 5. The path subcircuit 207a is constructed to include
18 one or more of the FETs, Q_{S1} and Q_{Sn} (as shown in Fig. 2A), each included FET representing
19 identified pass circuit elements of the worst case pull-up signal path. The sizes of the FETs included
20 in the path subcircuit 207 are based on the sizes of the respective pass circuit elements.

21 In step 303, a simulation is performed to determine the one margin ($V_{mar_{(1)}}$). An exemplary
22 embodiment of the simulation circuit 500 for the $V_{mar_{(1)}}$ determination is shown in Fig. 5. The $V_{mar_{(1)}}$
23 simulation circuit 500 includes the forward inverter portion, i.e., the complementary pair of FETs Q1
24 and Q2, the NFET Q3, the PFET Q6 and the path subcircuit 207a constructed in step 302 above. In
25 this exemplary simulation circuit 500, the FETs Q4 204 and Q5 205 shown in Fig. 2 are omitted.
26 However, in an alternative embodiment, the FETs Q4 204 and Q5 205 may be included, and turned
27 off.

1 The $V_{mar_{(1)}}$ simulation comprises a DC analysis of the simulation circuit 500 with the output
2 $V_{out\ 104}$ initially set to logical high, i.e., set to V_{DD} , and determining the voltage level at the input
3 terminal $V_{in\ 103}$. If the voltage level at the input terminal $V_{in\ 103}$ exceeds the V_{trip} , and is sufficiently
4 high to overcome the NFET Q3 203, the state of the output, $V_{out\ 104}$, would switch from the high
5 initial setting to a logical low. The one margin, $V_{mar_{(1)}}$, is the difference of the voltage level at $V_{in\ 103}$
6 and V_{trip} , i.e., $V_{mar_{(1)}} = V_{in} - V_{trip}$.

7 In step 304, the worst case pull-down signal path and the path subcircuit 207 based on the
8 worst case pull-down signal path are found as previously described. In particular, in an embodiment
9 of the present invention, the worst case pull-down signal path is determined analytically by traversing
10 through each of possible signal paths from the input of the latch to each of pull-down driver circuit
11 elements that can drive a pull-down signal to the input of the latch, and identifying pass circuit elements
12 along each of the signal paths, through which the pull-down signals may pass. For each of identified
13 pass circuit elements, a weight is applied to its resistance, e.g., based on its length and width (L/W).
14 The weights applied to the resistance of the pass circuit elements are empirically determined based on
15 the topology configuration of each of the circuit elements, e.g., the pass circuit element type (e.g.,
16 whether the pass circuit element is a single NFET, single PFET or a complementary pair of FETs), the
17 signal being passed through the pass circuit element and whether a threshold voltage drop occurs
18 between the pull-down driver circuit element and the pass circuit element.

19 The weighted resistance of the identified pass circuit elements along a particular signal path are
20 added together to determine a cumulative resistance of the particular signal path, i.e., from the ground
21 (GND) through the pull-down driver circuit element and the pass circuit elements to the latch input.
22 The cumulative resistance of each signal path is compared to the total resistance similarly calculated for
23 other pull-down signal paths to determine the worst case pull-down signal path, i.e., the signal path with
24 the highest cumulative resistance.

25 The pull-down driver of the identified worst case pull-down signal path is mapped to an
26 equivalent canonical driver circuit Q5 206 as shown in Fig. 5. The path subcircuit 207b is constructed
27 to include one or more of the FETs, Q_{S1} and Q_{Sn} (as shown in Fig. 2A), each included FET
28 representing identified pass circuit elements of the worst case pull-down signal path. The sizes of the

1 FETs included in the path subcircuit **207** are based on the sizes of the respective pass circuit elements.

2 In step **305**, a simulation is performed to determine the zero margin ($V_{mar_{(0)}}$). An exemplary
3 embodiment of the simulation circuit **600** for the $V_{mar_{(0)}}$ determination is shown in Fig. 6. The $V_{mar_{(0)}}$
4 simulation circuit **600** includes the forward inverter portion, i.e., the complementary pair of FETs Q1
5 and Q2, the NFET Q5, the PFET Q4 and the path subcircuit **207b** constructed in step **304** above.
6 In this exemplary simulation circuit **600**, the FETs Q3 **203** and Q6 **206** shown in Fig. 2 are omitted.
7 However, in an alternative embodiment, the FETs Q3 **203** and Q6 **206** may be included, and turned
8 off.

9 The $V_{mar_{(0)}}$ simulation comprises a DC analysis of the simulation circuit **600** with the output
10 V_{out} **104** initially set to logical low, i.e., set to ground, and determining the voltage level at the input
11 terminal V_{in} **103**. If the voltage level at the input terminal V_{in} **103** is below the V_{trip} , and is sufficiently
12 low to overcome the PFET Q4 **204**, the state of the output, V_{out} **104**, would switch from the low initial
13 setting to a logical high. The zero margin, $V_{mar_{(0)}}$, is the difference of V_{trip} and the voltage level at V_{in}
14 **103**, i.e., $V_{mar_{(0)}} = V_{trip} - V_{in}$. Finally, the process ends in step **306**.

15 If each of the one margin and the zero margin exceed a design guideline margin thresholds, the
16 circuit design is deemed acceptable, and proper operations of the latch is ensured.

17 As can be appreciated, the DC margin determination method described herein allows an
18 efficient and fast determination of DC margin of a latch without requiring numerous time consuming
19 simulations for each of the possible signal paths to the input of the latch.

20 Specific program listings for an embodiment of a method of determining the DC margin of a
21 latch in accordance with the principles of the present invention is provided in the Appendix, which
22 appears below.

23 While the invention has been described with reference to the exemplary embodiments thereof,
24 those skilled in the art will be able to make various modifications to the described embodiments of the
25 invention without departing from the true spirit and scope of the invention. The terms and descriptions
26 used herein are set forth by way of illustration only and are not meant as limitations. In particular,
27 although the method of the present invention has been described by examples, the steps of the method
28 may be performed in a different order than illustrated or simultaneously. Those skilled in the art will

- 1 recognize that these and other variations are possible within the spirit and scope of the invention as
- 2 defined in the following claims and their equivalents.
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